EECE 690/890
Digital Radio Hardware Design

Team 1
Assignment 1

Due 9/17/98

Introduction

This is the first of a series of assignments designed to guide you through the tasks needed to complete the RF transceiver design. Specific tasks are detailed below for each team member so that each person has a well-defined job and deliverable (material to be turned in by the due date). However, the tasks are also interdependent, so you need to work together.

Attached to this assignment is an additional page giving a preview of future tasks that will need to be completed before the PDR. You are encouraged to work ahead if you can. This will ease your workload when things like tests stack up in other classes in the coming weeks.

Transceiver Design Tasks

You should perform the following tasks:

- Download all of the data sheets for the transceiver and familiarize yourself with them.
- Create a spec summary sheet listing, for each IC, the important information you will need in the design, including at least the following:
  - Operating voltage range, and current consumption in each operating mode
  - Gain, Noise Figure, and Compression Point (input or output referenced)
  - Required minimum LO power levels for mixers
  - Input/output impedances
- Work with Synthesizer designer to decide on an operating voltage and expected current consumption from entire transceiver.

Your deliverables are listed below:

- A preliminary block diagram of the transceiver, including any filters you expect to use. Your block diagram should be in standard representation (like those in class), but should also show the ICs used. For example, you may want to draw a box around the LNA and first mixer to indicate that both are included in one IC. You can show the LOs as just a box called “synth”. The synthesizer designer will provide a separate block diagram for

these components. Show the VCO used as the TX modulator as a block. This circuit will actually be developed by the synthesizer designer, but it needs to be on this block diagram.

- Your spec summary sheet. If you like, you can annotate the block diagram with some of this information to show things like Gain, Noise Figure, etc. as we did in class/homeworks.
- An email message sent to your company's email list ("radioa-l" or "radiob-l") providing other members of the team with your assessment of voltage and power requirements. Note that this email should be done jointly with the synthesizer designer and should be for the entire transceiver.

Synthesizer Design Tasks

You should perform the following tasks:

- Download all of the data sheets for the synthesizer related circuits and familiarize yourself with them. You may have to work to get data on the varactor diodes since the Motorola site does not seem to have a single web page with this data.
- Create a spec summary sheet listing, for each IC, the important information you will need in the design, including at least the following:
  - Operating voltage range, and current consumption in each operating mode
  - Output power from LOs and input power required by synthesizer from LO
  - Input/output impedance levels
- Begin study of synthesizer PLL loop filter design discussed in class notes, and the two texts (Gardner and Hagen).
- From the LMX1602 data sheet, determine a value for the "phase detector constant" K_d (in Amperes/radian) that you will need later when you design your loop filter.
- Work with Synthesizer designer to decide on operating voltage and to specify expected current consumption from entire transceiver.

Your deliverables are listed below:

- A preliminary block diagram of the synthesizer.
- Your spec summary sheet.
- Your analysis of the phase-detector sensitivity.
- An email message sent to your company's email list ("radioa-l" or "radiob-l") providing other members of the team with your assessment of voltage and power requirements. Note that this email should be done jointly with the synthesizer designer and should be for the entire transceiver.

Team 1 Future Assignments

The following gives an overview of the tasks remaining after task 1. These will be broken down into assignments like task 1, with recommended subtasks and deliverables. We will also have periodic "mini-design reviews" in which your team will meet with the instructors. In these informal reviews, you will need to explain your design decisions, and we will try to find "holes" in the design that need to be addressed.

RF Transceiver Design

- Familiarize yourself with crystals, filters, and surface mount inductors available in manufacturers catalogs, and that we can get from distributors (see class web page).
- Estimate requirements for duplexer attenuation
- Work with synthesizer designer to develop a "frequency plan" (LO, IF frequencies, filter bandwidths, etc.).
- Select filters, etc.
- Design first IF filter if not available commercially
- Design demod circuits (like in EECE662)
- Draw "final" block diagram
- Draw "final" schematic
- Generate parts list for ordering components
- Do layout "floorplanning" (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic

Synthesizer Designer

- Complete study of loop filter transfer function design.
- Work with RF designer to define frequency plan
- Select crystals for synthesizer reference (may want to coordinate with Team 2)
- Decide on VCO tuning range / VCO constant

- Estimate loop bandwidth desired for PLL to guarantee reference spurs are < -60 dBc in alternate channel
- Do loop filter design
- Estimate worst-case lockup time given tuning range, loop filter, and VCO
- Work out divisors and other control settings to be programmed into LMX1602
- Supply information to software team (lockup time, divisors/controls, and hardware interface)
- Select varactor diode and design tuned circuit for LOs
- Design TX modulator VCO (see EECE662 notes)
- Draw schematics
- Generate parts list for ordering components
- Do layout “floorplanning” (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic