EECE 690/890
Digital Radio Hardware Design

Team 1
Assignment 2

Due Dates:

Informal Mini Design Review Thursday, 9/24/98
Written Deliverables Tuesday, 9/29/98

Introduction

This is the second of the series of assignments designed to guide you through the tasks needed to complete the RF transceiver design. Specific tasks are detailed below for each team member.

This time, there are two due dates. On, or around Thursday, 9/24 we will meet to go over your design in an informal miniature design review. Hence, you need to have most of the tasks completed by that date, with the exception of documentation. If you have problems, or questions, bring them to the design review. However, the main purpose of the review is for you to explain your current design (using the blackboard and any drawings, data sheets, etc that you wish to bring) and let your manager help you look for potential problems. Following this review you can make any needed changes before delivering the final written deliverables for this assignment.

Transceiver Design Tasks

You should perform the following tasks. Note that they are not necessarily sequential. You should work on all of these at the same time.

- Familiarize yourself with crystals, filters, and surface mount inductors available in manufacturers catalogs, and that we can get easily (i.e. quickly) from distributors. It is highly recommended that you look first at the distributor catalogs to help narrow your search. Our primary vendors are Digi-Key and Newark (see class web page). If necessary, we can try to track down parts that are not carried by these vendors. If you wish to consider this, see Steve or Joe downstairs in Rathbone 41.
- Estimate requirements for duplexer attenuation. This is similar to what was done in the first homework, and should not take long. However, you will need to look up the actual component specs rather than using the numbers given from the homework.

- Work with synthesizer designer to develop a "frequency plan" (LO, IF frequencies (~45 MHz and 10.7 MHz are recommended), filter bandwidths, etc.). This will be driven strongly by available filters and crystal frequencies, except at the first IF where you may need to create your own filter. Carefully consider the image responses you will encounter and make sure your filters can attenuate these frequencies sufficiently. For the first downconversion, remember that the image-reject mixer used in the downconverter IC provides some rejection. The rest will have to be made up by the filtering. For the second downconversion, the problem should be relatively easy since the preselect filter has already attenuated any RF signal that would cause an image response here. (What first IF frequency will create an image? What RF frequency does this correspond to? How much attenuation can you expect from the preselect filter at this RF frequency?) Hence, you should not need a very high Q or high order filter here. Also, think carefully about how the base and mobile units will differ. If one transmits on frequency f_1 and receives on f_2, then the other must tranmit on f_2 and receive on f_1. How does this impact your design?
- Select filters, and crystals. Remember that there are crystal oscillators needed elsewhere in the system. Could the entire phone work off a single crystal reference? What are the pros and cons of doing that? You will need to work with the synthesizer designer as well as the other teams in your company to decide this.
- Design first IF filter if not available commercially. Hopefully, the design requirements for this will work out to be easy as mentioned above. You may only need a single pole response. However, depending on impedance levels, the needed L and C values may or may not be realizable. Review your EECE662 notes here. If necessary, you could design a filter to work at a different impedance level and put matching networks at the input, output, or both. This is a commonly used strategy in RF circuit design to make component value more practical. Finally, remember that

Your deliverables are listed below:

- Your analysis of the duplexer requirements, and your analysis that shows that your selected preselect filter will work.
- Your frequency plan. Show this by placing frequencies and filter bandwidths on a block diagram drawing of the transceiver. Also, provide your analysis of image rejections and of any other issues you considered.
- A schematic for your first IF filter, together with a description of your design procedure.
- A parts list for the filters, crystals (if any), and first IF filter components. This should include both the manufacturer's part number and the vendor name and part number.

Synthesizer Design Tasks

You should perform the following tasks:

- Complete your study of loop filter transfer function design.
- Work with RF designer to define frequency plan. Remember that you will be implementing the TX VCO used for the FSK modulator. It is important that this VCO be temperature stable, so that places some constraints on the frequency you can use. (Assume LC components with 50 ppm/^{o}C drift). Also, it is very important that you consider how the transmit and receive frequencies relate. Remember that we will be using frequency duplex. Will you use the full dual-synthesizer and 2 RF VCOs, or is it possible to make a frequency plan where you can have a single RF VCO and synth? Also, think carefully about how the base and mobile units will differ. If one transmits on frequency f_1 and receives on f_2, then the other must tranmit on f_2 and receive on f_1. How does this impact your design?
- Select crystals for synthesizer reference (if any), or explain where you will get the reference frequency from.
- Decide on VCO tuning range / VCO constant. Remember that your L and C values will have tolerances, and that you must provide a frequency range sufficient to address this problem. You don't want manufacturing to have to "pre-align" each VCO. That would not be cost competitive. Also remember that you may need to make two different VCOs.
- Do loop filter design. For a first cut design, use about 1 kHz as the loop bandwidth. You can always modify this later if your analysis of lockup time, etc. turns out to not provide the needed system performance.
- Estimate worst-case lockup time given tuning range, loop filter, and VCO constants. To do this, assume that when the loop is not locked, the phase/frequency detector puts out pulses with about a 50% duty cycle in the proper polarity to slew the frequency toward that needed. Take the average current from the phase detector and see how long this must be supplied to the capacitor before the cap charges to the required voltage. To get a worst-case lockup time, assume that the cap is initially uncharged. What voltage should you assume that it needs to charge to? For our phone, a lockup time in the neighborhood of about 10 ms is probably OK. If your time comes out greater than this, consider widening the loop bandwidth and redesigning the loop filter. However, remember that the loop bandwidth needs to be << the reference frequency to prevent the phase correction pulses from modulating the VCO frequency.

Your deliverables are listed below:

- Your frequency plan. Show this by placing frequencies and filter bandwidths on a block diagram drawing of the transceiver. Provide a discussion of what the synthesizer RF and reference frequencies will be at both the base and mobile, and if you plan to use a shared VCO for both the TX and RX, prove that this will work. Also, support your choice of a

TX modulator frequency with an analysis/discussion of expected frequency drift with temperature.

- Documentation of your VCO tuning range requirements showing how you will address manufacturing tolerances on L and C values, and how you will address the difference in the TX and RX frequencies if you are using a dual synthesizer transceiver architecture.
- Documentation explaining your loop filter design, including as a minimum, a schematic showing your component values and a summary of your transfer function analysis. This should clearly show the major values involved in the design: R, C, phase-detector constant, VCO constant, divide ratio N, and transfer function Q and omega values.
- Your lockup time analysis and result.

Team 1 Future Assignments

The following gives an overview of the tasks remaining after task 2.

RF Transceiver Design

- Design demod circuits (like in EECE662), plus the data slicer circuit
- Draw “final” block diagram
- Draw “final” schematic
- Generate parts list for ordering components
- Do layout “floorplanning” (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic

Synthesizer Designer

- Work out divisors and other control settings to be programmed into LMX1602
- Supply information to software team (lockup time, divisors/controls, and hardware interface)
- Select varactor diode and design tuned circuit for LOs
- Design TX modulator VCO (see EECE662 notes)
- Draw schematics
- Generate parts list for ordering components
- Do layout “floorplanning” (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic