EECE 690/890
Digital Radio Hardware Design

Team 1 Assignment 3

Due Date: Tuesday, 10/13/98

Introduction

This is the third in a series of assignments designed to guide you through the tasks needed to complete the RF transceiver design. Specific tasks are detailed below for each team member.

This time, there are two due dates. On, or around Thursday, 9/24 we will meet to go over your design in an informal miniature design review. Hence, you need to have most of the tasks completed by that date, with the exception of documentation. If you have problems, or questions, bring them to the design review. However, the main purpose of the review is for you to explain your current design (using the blackboard and any drawings, data sheets, etc that you wish to bring) and let your manager help you look for potential problems. Following this review you can make any needed changes before delivering the final written deliverables for this assignment.

Transceiver Design Tasks

You should perform the following tasks.

- Design demod circuits. For this, you should review your EECE662 notes. Recall that our data rate is 96 kb/s and our FSK bandwidth will be on the order of 200 kHz. Hence, you should make sure the Q of your quadrature circuit is > 200 kHz. The chip used here should be similar to that you used before, but you should refer to the data sheet for specific recommendations on the design.
- Design the data slicer circuit. You should use considerations similar to those in homework 4, but note that the settling time given in that homework was unrealistically long. Use the settling time requirement determined in homework number 5. Also, note that the open collector output stage comparator suggested in the homework is probably not a good choice. You should select a different comparator for this - one with a voltage output (push-pull stage) that will not draw static current (other than the quienscent DC current of the device) when in the low state. In addition, since it will not have a power-down option (most likely), it should be a low power device. Finally, you should select a dual comparator device, since you will need a comparator to do the signal-present detector design in the following item.

- Study the RSSI circuit in the SA636 data sheet and design a suitable circuit to output a logic high if the signal detected is > -80 dBm, and a zero otherwise. You may want to make this adjustable, especially if the data sheet does not give tight tolerances on what the RSSI level will be for this signal power.
- Draw a "final" block diagram and a final schematic. You should probably work with your teammate on this.
- Generate a parts list for ordering components. The parts list should give quantity, manufacturers part number, vendor, vendor part number, price each, and price total. You do not need to include discrete resistors or capacitors, unless they are unusual values that we do not have in the comm lab.

Your deliverables are listed below:

- Your design notes on the demod, data slicer, and RSSI circuits.
- Your block diagram and schematic.
- Your parts list.

Synthesizer Design Tasks

You should perform the following tasks:

- Work out divisors and other control settings to be programmed into LMX1602. Put yourself in the place of the software engineer trying to send all the necessary bits to the synthesizer, for a) initialization, and b) frequency updates as the channels are scanned. Some registers probably only need to be programmed once (e.g. the reference divider value and some configuration bits) during the initialization, while others need to be updated whenever the frequency is changed. Give the programming words needed for each channel and each synth (if you are using different frequencies in different synths).
- Think about testing too! You may want to supply the software team with bit settings that will place the monitor pins in the synth into various modes like outputing the divided down reference, outputting the divided down VCO, etc. so that when the thing doesn't lock up, you can find out what's going on!
- Supply the above information to software team in an email message.
- Select a varactor diode and design tuned circuit for LOs.
- Design a (low power) TX modulator VCO (see EECE662 notes). You probably want a common-base Colpitts oscillator here for simplicity. Determine a reasonable sensitivity to give the desired peak deviation. You may want to design for peak deviation with a 1 Vp-p digital input rather than a 5Vp-p value to provide better linearity. If so, design a

voltage divider to drop the digital swing down to this level. Remember that you will need to align your VCO also, so include an appropriate variable cap in addition to your varactor used for modulation. Finally, add a 'pad' at the output to allow adjusting the output level, or prototype the circuit in the lab and design for the proper output level into the TX upconverter IC.

- Draw a "final" block diagram and a final schematic. You should probably work with your teammate on this.
- Generate a parts list for ordering components. The parts list should give quantity, manufacturers part number, vendor, vendor part number, price each, and price total. You do not need to include discrete resistors or capacitors, unless they are unusual values that we do not have in the comm lab.

Your deliverables are listed below:

- A copy of your synthesizer programming information supplied to Team 3.
- Your design notes on the LO and TX VCO circuits.
- Your block diagram and schematic.
- Your parts list.

Team 1 Future Assignments

The following gives an overview of the tasks remaining after task 2.

RF Transceiver Design

- Do layout “floorplanning” (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic

Synthesizer Designer

- Do layout “floorplanning” (best placement of parts on board)
- Do layout and supply to team 4
- Do test planning and add test points to block diagram and schematic