

# EECE 690/890

## Digital Radio Hardware Design

### Team 2

### Assignment 2

**Due 10/1/98**

#### Introduction

This is the second of a series of assignments designed to guide you through the tasks needed to complete the PLC/ADPCM design. Specific tasks are detailed below for each team member so that each person has a well-defined job and deliverables (material to be turned in by the due date). However, the tasks are also interdependent, so you need to work together.

Now that you have learned how to use the Altera software and designed the first primitive that we need to finish the digital part of the cordless phone, we can design, build and test parts of the PLD. Team two members should now have there specific task in hand and there should not be anything in our way to be complete our part.

Attach to this assignment is a block-diagram for the Rx- and Tx-PLD that will assist you in design of the PLD.

#### RX-PLD/ADPCM Design Tasks

You should perform the following tasks:

- Design, build and test a bit synchronizer according to following specifications.
- Design a state machine that will have

Present state					Next State				
S3	S2	S1	S0	A	S3	S2	S1	S0	
• 0	0	0	0	0	0	0	0	1	
• 0	0	0	0	1	0	0	0	0	
• 0	0	0	1	0	0	0	1	0	
• 0	0	0	1	1	0	0	0	0	
• 0	0	1	0	0	0	0	1	1	
• 0	0	1	0	1	0	0	0	0	
• 0	0	1	1	0	0	1	0	0	
• 0	0	1	1	1	0	0	0	0	
• 0	1	0	0	0	0	1	0	1	
• 0	1	0	0	1	0	0	0	0	
• 0	1	0	1	0	0	1	1	0	
• 0	1	0	1	1	0	0	0	0	

•	0	1	1	0	0	0	1	1	1
•	0	1	1	0	1	0	0	0	0
•	0	1	1	1	0	1	0	0	0
•	0	1	1	1	1	0	0	0	0
•	1	0	0	0	0	1	0	0	1
•	1	0	0	0	1	0	0	0	0
•	1	0	0	1	X	0	0	1	0
•	X	X	X	X	X	0	0	0	0

- Enable active low.
  - Reset active low.
  - Put your design into a symbol.
- Design, build and test the Rx-queue according to following specifications.
    - The Rx queue should be serial in and parallel out (Use your previous design).
    - Queue size 4+16+4, there is no need to store the preamble.
    - Enable active low.
    - Reset active low.
    - Put your design into a symbol.

Your deliverables are listed below:

- For the bit synchronizer.
  - Your design.
  - Complete schematic of the bit synchronizer.
  - Your test schematic (With the symbol in it).
  - Test results.
- For the RX-queue.
  - Your design.
  - Complete schematic of the Rx-queue.
  - Your test schematic (With the symbol in it).
  - Test results.

## TX-PLD/ADPCM Design Tasks

You should perform the following tasks:

- Design, build and test the Tx-queue according to the following specifications.
  - The queue should be parallel in and serial out.
  - The queue size should be 16+4+16+4.
  - Enable active low.
  - Reset active low.
  - Put your design into a symbol.

- Design, build and test a multiplexer according to following specifications.
  - The output should be 40 bits long.
    - 16 bit (Preamble) + 4 bit (ID) + 16 bit (DATA) + 4 bit (CRC)
  - The preamble should have a direct path through (It is always in the frame).
  - The CRC bits should also have a direct path through (Also, always in the frame.)
  - The 4 bit ID always comes from Microcontroller and needs to have a direct path through the multiplexer.
  - Next 16 bits either comes from the Microcontroller or the ADPCM depending on the SELECT.
  - SELECT.
    - High if data from ADPCM and Low if data from the MICROCONTROLLER.
  - Enable active low.
  - Reset active low.
  - Put your design into a symbol.

Your deliverables are listed below:

- For the Tx-queue.
  - Your design.
  - Complete schematic of the Tx-queue.
  - The test schematic. (With your symbol in it).
  - Test results.
- For the Multiplexer.
  - Your design.
  - Complete schematic of the multiplexer.
  - The test schematic. (With your symbol in it).
  - Test results.