EECE 690/890
Digital Radio Hardware Design

Team 2
Assignment 3

Due 10/13/98

Introduction

This is the third of a series of assignments designed to guide you through the tasks needed to complete the PLC/ADPCM design. Specific tasks are detailed below for each team member so that each person has a well-defined job and deliverables (material to be turned in by the due date). However, the tasks are also interdependent, so you need to work together.

In this assignment we will continue to design the PLD that we need for the cordless phone to work properly. To achieve our goal we need to be absolutely sure that each member or team is designing a circuit that will integrate easily. For this reason, we will have a mini design review session either on the 8th (Thursday) or 9th (Friday) of October for each team. Each team will give a short presentation on their progress. We will also discuss vector analysis.

Following is the list of tasks and deliverables for each team member. Please notify Dr. Kuhn or Hafthor if there are any discrepancies in the assignments.

RX-PLD/ADPCM Design Tasks

You should perform the following tasks:

- Design a frame synchronizer that will identify a given pattern in the data stream (here 1111). When the frame synchronizer finds the given pattern, it will set a flag and disable itself. The flag will start a counter and enable the loading of the RX-queue. When the counter hits 20 it will reset the frame synchronizer and the count, and load the RX-queue data into the Micro-controller/ADPCM interfaces. The frame synchronizer will have four inputs: data stream (RX-data), clock, reset (asserted low), enable (asserted low) and two outputs: count enable (asserted low) and Load.

- Design a parallel to serial interface to the micro-controller.

  The interface will have

  A parallel load, asserted high (input).
  Data bus 20 lines (input).
  Clock (if you have synchronize parallel load) (input).
  Serial clock (input)

Enable (asserted low) (input)
Reset (asserted low) (input)
Serial Data (output)
Data ready, asserted high(latched output)
Latch clear, asserted low (output)

- Design a parallel to serial interface to the ADPCM (data path)

  The interface will have

  A parallel load (input).
  Data bus 16 lines (input).
  Clock (input)
  Enable (asserted low) (input)
  Reset (asserted low) (input)
  Serial Data (output)

Your deliverables are listed below:

- Your designs.
- Complete schematics or VHDL code.
- Your test schematics (With the symbol in it).
- Test results.

TX-PLD/ADPCM Design Tasks

You should perform the following tasks:

- Design a Tx-sequencer . Design a counter that will count 0-47-0... and output a HIGH in count 1 and LOW everywhere else. The output will cause the queue to be loaded from the Micro-controller/ADPCM interface latches every 48 clocks. This device will have three inputs: clock, reset asserted LOW, enable asserted LOW and one output specified earlier.

- Design a serial to parallel interface to the micro-controller.

  The interface will have

  Serial in (input).
  Serial clock (input)
  Enable (asserted low) (input)
  Reset (asserted low) (input)
  Data bus 20 (output)
  Data ready (latched output)

Latch clear (output)

- Design a serial to parallel interface for the ADPCM (data path)

  The interface will have

  Serial in (input).
  Clock (input)
  Enable (asserted low) (input)
  Reset (asserted low) (input)
  Data bus 16 (output)

- Your deliverables are listed below:

  - Your designs.
  - Complete schematics or VHDL code.
  - Your test schematics (With the symbol in it).
  - Test results.