EECE 690/890
Digital Radio Hardware Design

Team 2
Assignment 4

Due 10/22/98

Introduction

This is the fourth of a series of assignments designed to guide you through the tasks needed to complete the PLC/ADPCM design. Specific tasks are detailed below for each team member so that each person has a well-defined job and deliverables (material to be turned in by the due date). However, the tasks are also interdependent, so you need to work together.

In this assignment we will design the rest of the building blocks for the PLD. After verifying the functionality of each component, we will put them together and attempt to simulate each section (RX or TX) independently. After ALL this is done and it seems to work, you and your partner are required to draw a complete block diagram of the PLD and make a table that will specify all signals needed for the PLD. Both the block diagram and the input/output sheet will be given to team 3 and 4 for further utilization . Therefore, it is very important that both the block diagram and the input/output sheet be as accurate as possible.

RX-PLD/ADPCM Design Tasks

You should perform the following tasks:

Design Rsync generator that will have:

- A clock cycle of 8 KHz and synchronized to the trailing edge of Bclock.
- Enable asserted low.
- Reset asserted low.
- Make sure that you study the data sheet for the ADPCM.

Design a ADPCM data loader that will:

- Stay high for five Bclock pulses and low for the rest of the cycle, starting on the rising edge of Rsync.
- Enable asserted low.
- Reset asserted low.
- Make sure that you study the data sheet for the ADPCM.

Design a RX-PLD:

- Put all the component that we have been design together on one schematic.
- Compile and simulate.
- Functionally test the RX-PLD (Convince your CEO that it will work).

Draw a complete block diagram of the RX part.

Make a table (on a separate page) of all signals that the PLD needs. This sheet will be given to both team 3 and team 4, so be complete. Note, there should only by one sheet per team.

Your deliverables are listed below:

- Schematic for both the RSYNC and ADPCM LOADER.
- Schematic for the RX-PLD
- Test circuit and results.
- Block diagram.
- Table of input/output specification for the PLD.

TX-PLD/ADPCM Design Tasks

You should perform the following tasks:

Design Xsync generator that will have:

- A clock cycle of 8 KHz and synchronized to the trailing edge of Bclock.
- Enable asserted low.
- Reset asserted low.
- Make sure that you study the data sheet for the ADPCM.

Design a ADPCM data loader that will:

- Stay high for five Bclock pulses and low for the rest of the cycle, starting on the rising edge of Xsync.
- Enable asserted low.
- Reset asserted low.
- Make sure that you study the data sheet for the ADPCM.

Design a CRC that will:

- This is a dummy block.

- Will have 8 outputs all tied to low.
- Enable asserted low.
- Reset asserted low.

Design a Preamble that will:

- Block that outputs the fixed preamble.
- Enable asserted low.
- Reset asserted low.

Design a TX-PLD:

- Put all the component that we have been design together on one schematic.
- Compile and simulate.
- Functionally test the TX-PLD (Convince your CEO that it will work).

Draw a complete block diagram of the TX part.

Make a table (on a separate page) of all signals that the PLD needs. This sheet will be given to both team 3 and team 4, so be complete. Note, there should only by one sheet per team.

Your deliverables are listed below:

- Schematic for both the XSYNC, ADPCM LOADER, CRC and PREAMBLE.
- Schematic for the TX-PLD.
- Test circuit and results.
- Block diagram.
- Table of input/output specification for the PLD.