# EECE 690/890
# Digital Radio Hardware Design

## Team 2
## Assignment 5

## Demo due 11/23/98
## Documentation due 12/3/98

**Introduction**

This is the fifth of a series of assignments designed to guide you through the tasks needed to complete the PLC/ADPCM design. Specific tasks are detailed below for each team member so that each person has a well-defined job and deliverables (material to be turned in by the due date). However, the tasks are also interdependent, so you need to work together.

At this point each team should have a working RX/TX PLD. But before you can program the actual chip and test, you and your partner need to fix few design problems. Up to this point we have assumed that the master clock (8xclock) would be given to the PLD design team from an outside source. The first part of this assignment is to solve this dilemma and generate the master clock internally. This will be accomplished by taking the 10.368 MHz clock from the ADPCM and dividing it approperly. The master clock (8xclock) should be 8x96kHz or 786 kHz. This means that we need to divide the 10.368 MHz first by 10.368 MHz / 786 kHz or 13.19, a problem. To fix this problem we are going to change the bit-synchronous so it will effectively divide by 9. By doing so we can divide the 10.368 MHz by 12 to get 864 kHz and then by 9 to get 96 kHz. The pre-scaler can be implemented on either or both the TX/RX chip. After you and your partner have fixed all the problems, you can program the chip according to pin allocation given by team 4. If there are any problem with fitting or missing pins that need to be used on the chips, please notify team 4 about the changes. After you have successfully program the chips you are to place your design in the test bench* and verify that it really work… GOOD LUCK… Remember that this is a team assignment.

* Documentation will be provided by Dr. Kuhn and Mr. Hafthor…

**RX-PLD/ADPCM - TX-PLD/ADPCM Design Tasks**

You should perform the following tasks:

- Modify bit-synch circuit.
- Design Pre-scaler (Divide 12).
- Program the chips.
- Verify design in test bench.

Your deliverables are listed below:

- Hard copy of all Schematic in the PLD (Due at Demo).
- Electronic copy of all design with documentation (On a floppy).
- Demo the circuit to Dr. Kuhn and Mr. Hafthor.